FORMING JFET AND LDMOS TRANSISTOR IN MONOLITHIC POWER INTEGRATED CIRCUIT USING DEEP DIFFUSION REGIONS

BACKGROUND OF THE INVENTION

[0001] Monolithic power integrated circuits (PICs) for high-voltage applications may sometimes integrate thereon a junction field effect transistor (JFET) and a lateral double-diffused metal-oxide-semiconductor (LDMOS) transistor. For instance, a JFET device may be incorporated in a power integrated circuit to use as a normally on pass device for a startup circuit. The JFET device may have a drain terminal connected to a power source terminal (e.g. 12V), a gate terminal that is grounded, and a source terminal connected to a power supply node for a load. As the power source ramps up, the JFET conducts current in a channel between the drain and the source terminal to provide power to certain circuitry of the load. When the power supply node (source terminal) to the load reaches the desired power supply voltage for the load (e.g. 5V), the JFET channel is pinched off and the JFET device is turned off. JFET devices are preferred in the normally on pass device application because of their good pinch off characteristic which ensures that circuitry downstream to the source terminal of the JFET is protected from the high voltage of the power source.

[0002] Meanwhile, LDMOS transistors are commonly used in high-voltage applications (20 to 500 volts) because of their high breakdown voltage characteristics and compatibility with CMOS technology for low voltage devices. In general, an LDMOS transistor includes a polysilicon gate, an N+ source region formed in a P-type body region, and an N+ drain region. The N+ drain region is separated from the channel formed in the body region under the polysilicon gate by an N drift region. It is well known that by increasing the length of the N drift region, the breakdown voltage of the LDMOS transistor can be accordingly increased.

[0003] When a JFET device and an LDMOS transistor are fabricated on the same integrated circuit, it is sometimes challenging to optimize the characteristics of both devices while maintaining a reasonably cost effective fabrication process. FIG. **1** is a cross-sectional view of a power integrated circuit including a JFET and an LDMOS transistor formed on the same semiconductor substrate in one example. When JFET **1** and LDMOS device **2** are manufactured using the same fabrication process, the devices have to be formed using the same diffusion regions available in the fabrication process. In particular, the traditional method for integrating a JFET into a LDMOS fabrication process uses the P-type body (P-body) region **4** of the LDMOS to form the gate region. However, the P-body implant is tailored for the threshold voltage in the channel and the breakdown voltage rating of the LDMOS transistor. The same P-body implant used as the gate region for the JFET device may not yield the desired pinch-off voltage to pinch off the transistor channel. For example, when the P-body implant is optimized for the LDMOS transistor threshold voltage and breakdown voltage, the JFET device may end up with a threshold voltage of 20V or more to pinch off the JFET conduction channel which is undesirable in the case where the JFET is coupled to supply circuitry operating at 5 volts. It is thus difficult to optimize both the JFET device and the LDMOS transistor in a power integrated circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] Various embodiments of the invention are disclosed in the following detailed description and the accompanying drawings.

[0005] FIG. **1** is a cross-sectional view of a power integrated circuit including a JFET and an LDMOS transistor formed on the same semiconductor substrate in one example.

[0006] FIG. **2** is a cross-sectional view of a power integrated circuit including a JFET and an LDMOS transistor formed on the same semiconductor layer according to embodiments of the present invention.

[0007] FIG. **3** is a cross-sectional view of an LMOS transistor in a power integrated circuit according to embodiments of the present invention.

[0008] FIG. **4** illustrates a non-isolated LDMOS transistor formed in the same manner as the LDMOS transistor of FIG. **3** with the N-type buried layer omitted in some embodiments of the present invention.

DETAILED DESCRIPTION

[0009] The invention can be implemented in numerous ways, including as a process; an apparatus; a system; and/or a composition of matter. In this specification, these implementations, or any other form that the invention may take, may be referred to as techniques. In general, the order of the steps of disclosed processes may be altered within the scope of the invention.

[0010] A detailed description of one or more embodiments of the invention is provided below along with accompanying figures that illustrate the principles of the invention. The invention is described in connection with such embodiments, but the invention is not limited to any embodiment. The scope of the invention is limited only by the claims and the invention encompasses numerous alternatives, modifications and equivalents. Numerous specific details are set forth in the following description in order to provide a thorough understanding of the invention. These details are provided for the purpose of example and the invention may be practiced according to the claims without some or all of these specific details. For the purpose of clarity, technical material that is known in the technical fields related to the invention has not been described in detail so that the invention is not unnecessarily obscured.

[0011] In embodiments of the present invention, a method to form JFET and LDMOS transistor devices in a monolithic power integrated circuit uses the LDMOS body region to form the JFET gate region and further uses a deep diffusion regions formed under the body regions to optimize the electrical characteristics of both the JFET and the LDMOS devices. The deep diffusion regions have the same dopant conductivity type as the body region and are more heavily doped. In some embodiments, the deep diffusion regions may be formed using a single mask implantation process. Accordingly, the LDMOS body region is optimized for the desired threshold voltage and breakdown characteristics of the LDMOS transistor. Meanwhile, the deep diffusion regions are used to optimize the pinch-off voltage for the JFET device and also to reduce the on resistance (Rds-A) and to improve the reliability of the LDMOS transistor device. In this manner, a single deep diffusion process is used to optimize both the JFET device and the LDMOS transistor device.

[0012] In the present description, a junction field-effect transistor (JFET) refers to a semiconductor device where